Monolithic 6W Ka-Band High Power Amplifier

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***Abstract* — The design and performance of a fully monolithic 6W Ka-band power amplifier is outlined. Excellent agreement between modeled and measured performance was demonstrated. This 3-stage power amplifier, which power combines 16 FET's on the third stage, is fully matched on chip to 50Ω at the input and output wire bond pads. Performance achieved ~20.5dB gain from 24-32 GHz with a peak power of >6W and PAE of ~21%. This performance was achieved using a 0.1um Power PHEMT process. To the authors knowledge, this is the highest output power demonstrated from a single device in this frequency band [1]-[5].**

I. Introduction

Commercial application in the Ka-Band have driven the development of power amplifiers with increased electrical performance in the areas power, gain and efficiency, among others. Emerging commercial applications with the potential for significant volume have also resulted in significant efforts to drive down the cost of these components. Many of these applications have a need for power levels as high as 10W or more in order to provide the link margin necessary for the system to function properly. When achieving these levels of power (at these frequencies) there is always a trade off between using a larger Monolithic Microwave Integrated Circuits (MMIC's) with greater power to minimize the number of devices that must be combined or power combining a larger number of lower power devices. The best approach for this will depend, of course, on many issues which must be traded. Inevitably the lowest cost solution is the most likely to be used. The power amplifier described here is clearly one that would be used to minimize the number of devices that must be power combined at the module level. The cost of this device in production quantities has not yet been determined but is still clearly a step forward in the demonstration of the power levels that can be achieved on a single chip at Ka-Band. The design of this amplifier was completed in August 1998. Measurements confirming the results were completed in October 1999.

II. Process Selection

Though cost is always important to us, it was not the main driver in this design. We selected an advanced Power PHEMT process and entered into an agreement for a cooperative research program. A 0.1um power PHEMT process was selected for this effort.

II. Circuit Design

Active and passive device models were developed by Motorola and verified by measurement if test structures were available otherwise electromagnetic simulation was used. FET models were based on a 300um FET and scaled to the peripheries used in the design. The third stage is implemented using sixteen 920um FET's. The second stage and first stages use eight and four 1050um FET's, respectively. This results in the 3rd, 2nd and 1st stages having total peripheries of 14.72mm, 8.4mm and 4.2mm respectively. The optimum load line for class A biasing was selected using load pull data.

Stability of the circuit and combining losses were examined very closely from the start. After the peripheries of the three stages were chosen, the output network was synthesized with the goal of minimizing the combining losses using a combination of electromagnetic and circuit simulations. The output combining structured used has a simulated loss of about 0.7 dB with a broadband impedance of 50Ω at the RF output bond pad.

All high frequency bias bypassing and stability was accomplished using on chip components. Unconditional stability was demonstrated by simulation for the full circuit as well as the individual stages and some sub-circuits. Low frequency bypassing was accomplished using off chip 100pF capacitors.

Interstage matching was implemented so that a broadband flat gain response could be achieved while making sure the power match and periphery of the driver stages was

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sufficient, with margin, to avoid early compression of the driver stages.

The input structure was synthesized to provide flat gain with a broadband 50Ω impedance at the input bond pad.

Thermal and stress analysis were also completed to insure that there were no issues.

A photograph of the 6W power amplifier is shown in Figure 1.

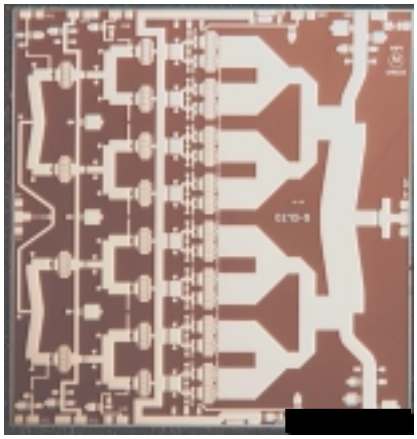

Fig. 1.Photograph of the Ka-Band HPA MMIC. This size of this MMIC is 26.3mm^2.

III. Measured Performance

The MMIC's were evaluated with on-wafer testing. Configuration of the test set was made with thermal issues being eliminated by use of proprietary techniques.

Excellent agreement between modeled and measured small signal performance was demonstrated. Figure 2 shows the small signal modeled performance along with the measured small signal gain of two HPA's. In this figure the red curve is the predicted small signal gain with and the measured performance of two MMIC's. Measured performance indicates about 21.5 dB of gain from 25 to 31 GHz.

A comparison was also made between predicted input return loss and measurement. Figure 3 shows the predicted input return loss. The predicted result was about 10dB return loss over the band with a measured performance of about 8dB over the band.

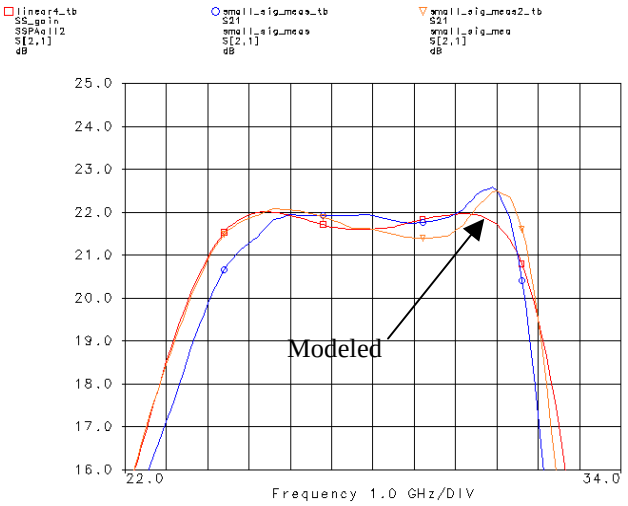

Fig. 2. Measured and modeled small signal gain of the Ka-Band HPA MMIC.

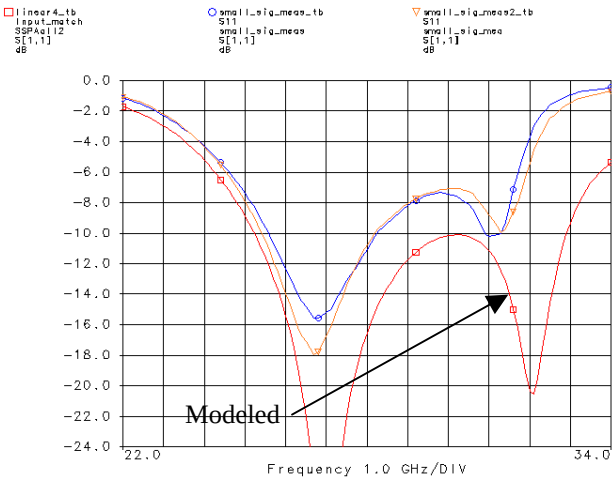

Fig. 3. Measured and modeled input return loss of the Ka-Band HPA MMIC.

Measured output power for the HPA MMIC is shown in Figure 4. The measurements demonstrate output power of >37 dBm from 29 to 31 GHz and >37.7 dBm from 30 to 31 GHz with +19dBm of input power.

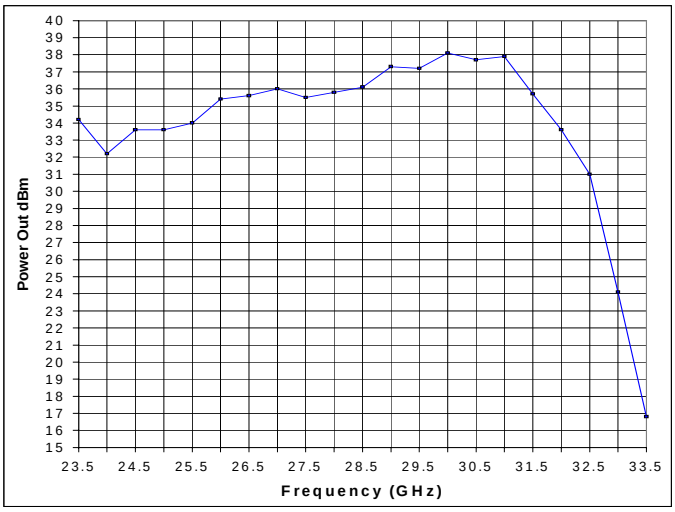

Fig. 4. Measured output power of the Ka-Band HPA MMIC with +19dBm of input power.

IV. ACKNOWLEDGEMENTS

The author would like to acknowledge the millimeter wave characterization support received from John Holmes from Motorola Labs, Motorola Inc.

V. SUMMARY

Power performance was demonstrated at a level that, to the author's knowledge, is the highest output power demonstrated to date from a single device at Ka-Band while achieving broadband flat gain. Additionally, excellent agreement between modeled and measured performance was described.

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